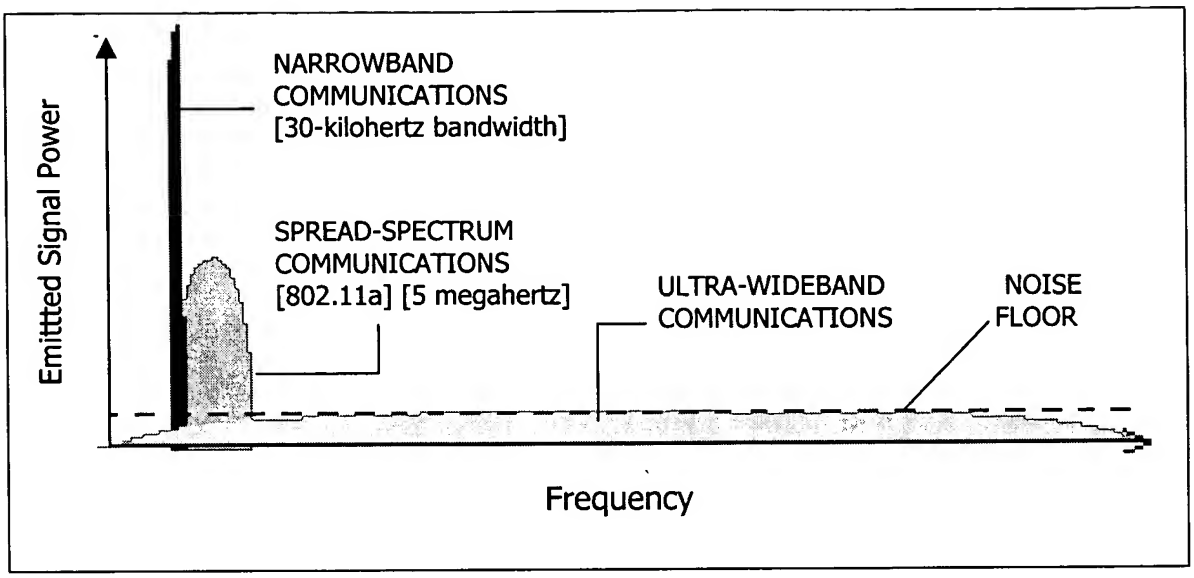


FIGURE 1

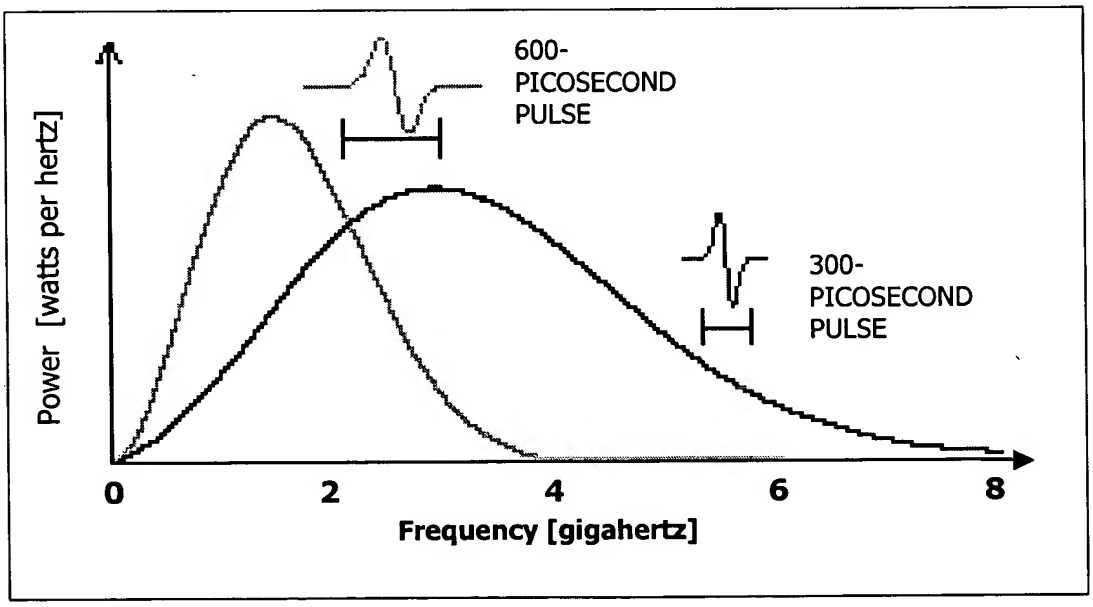


FIGURE 2

FIGURE 3

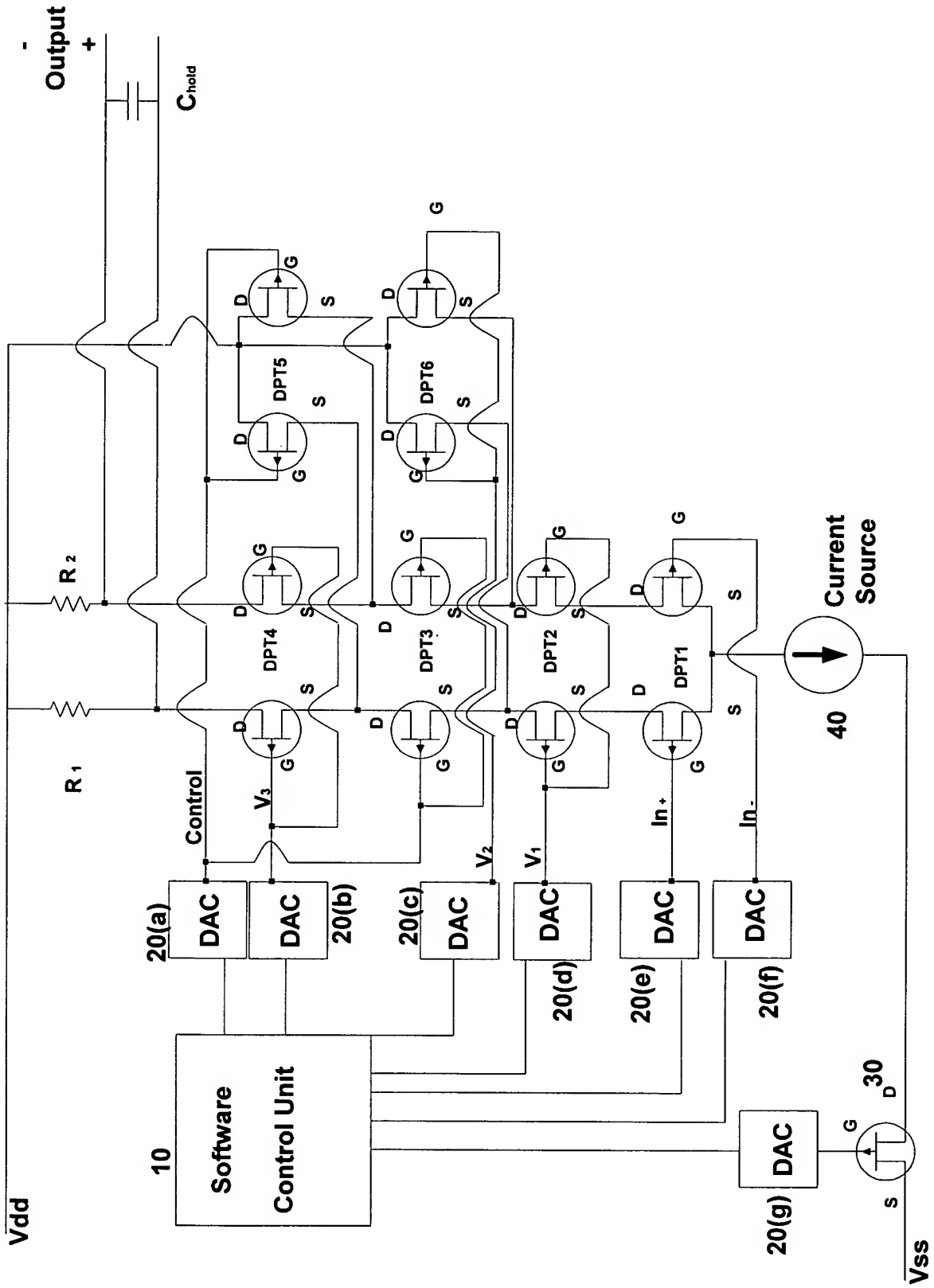

Output
-
+
C_{hold}
R_2
R_1
Vdd
Vss
DPT1
DPT2
DPT3
DPT4
DPT5
DPT6
D
G
S
Control
V_3
V_2
V_1
In_+
In_-
DAC
20(a)
20(b)
20(c)
20(d)
20(e)
20(f)
20(g)
10
Software
Control Unit
30
40
Current
Source

FIGURE 4

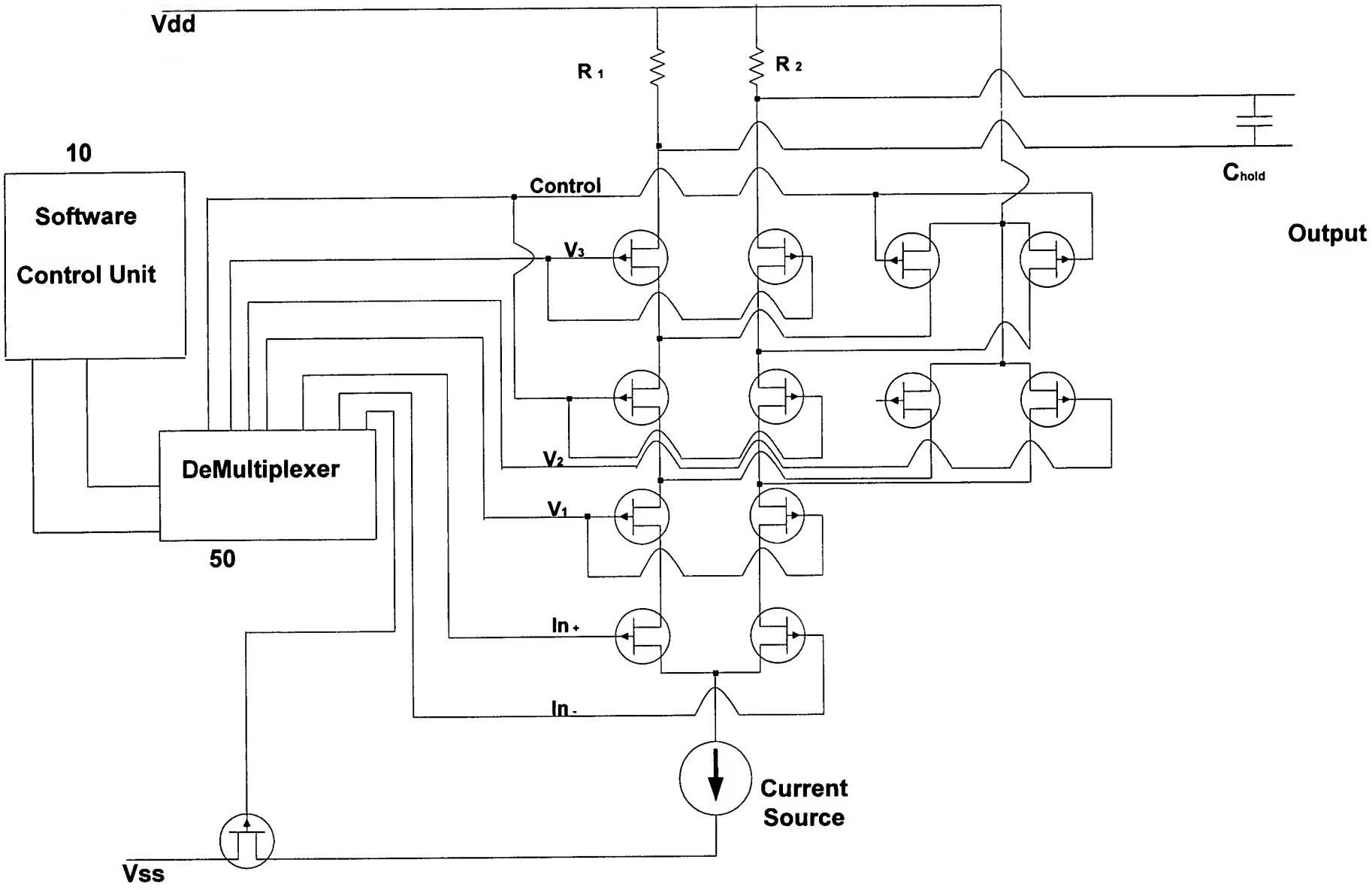

Vdd
R 1
R 2
10
Software
Control Unit
Control
V3
Chold
Output
V2
DeMultiplexer
50
V1
In +
In -
Current
Source
Vss

FIGURE 5

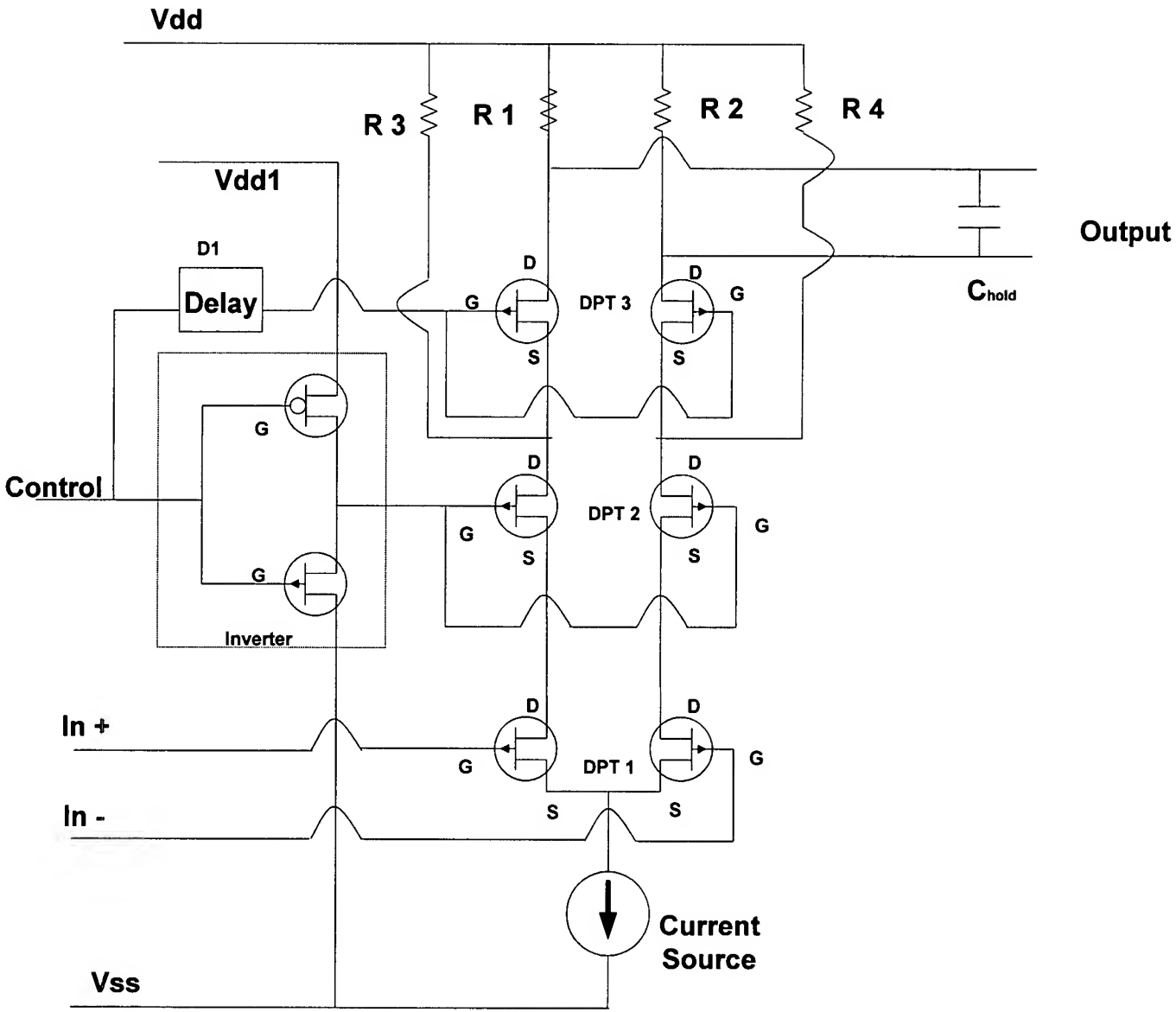

Vdd
R 3
R 1
R 2
R 4
Vdd1
D1
Delay
Output
C_{hold}
D
G
S
DPT 3
DPT 2
DPT 1
Control
Inverter
In +
In -
Current Source
Vss

FIGURE 6

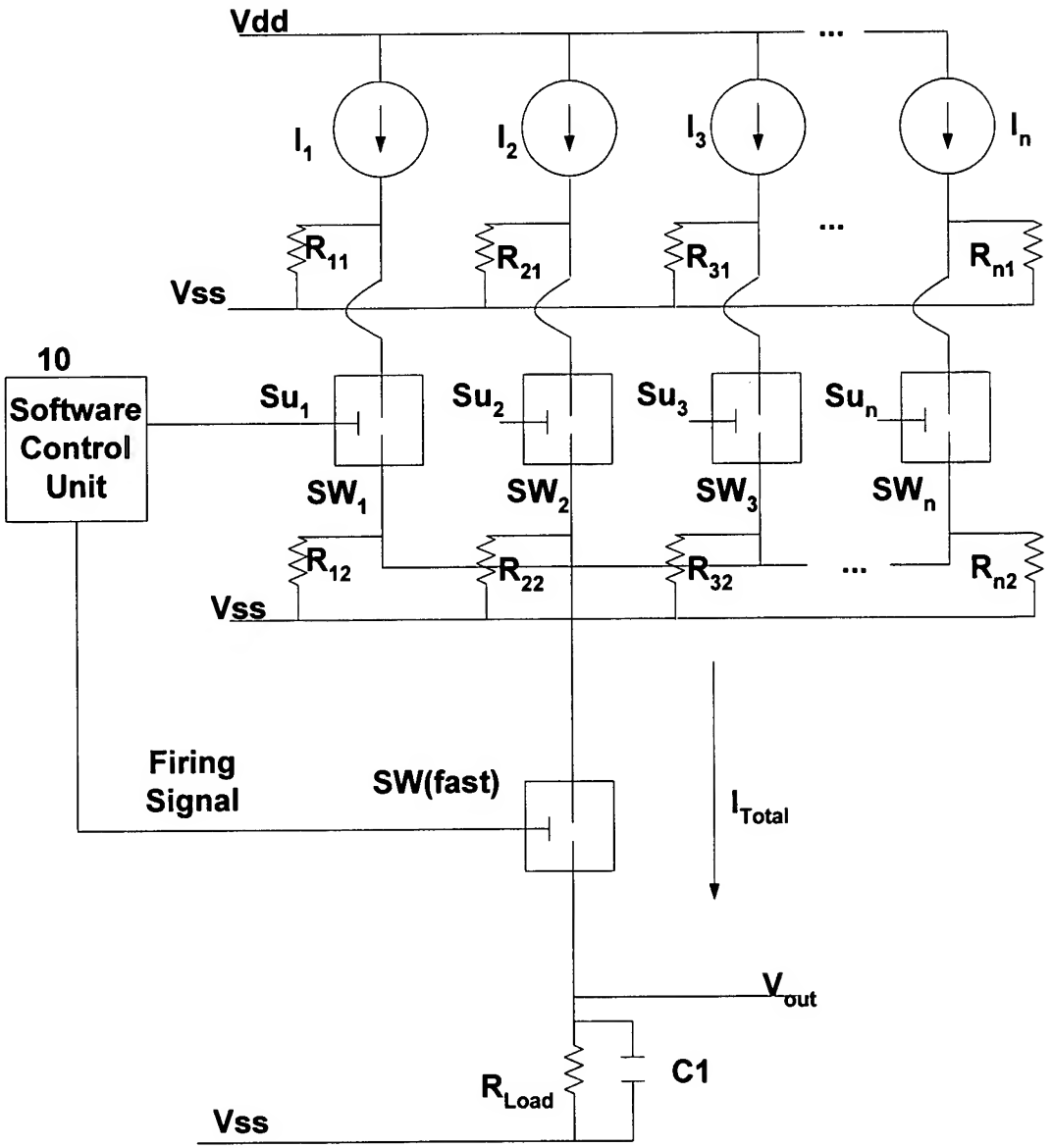

Vdd
...
I_1
I_2
I_3
I_n
R_{11}
R_{21}
R_{31}
R_{n1}
Vss
10
Software Control Unit
Su_1
Su_2
Su_3
Su_n
SW_1
SW_2
SW_3
SW_n
R_{12}
R_{22}
R_{32}
R_{n2}
Vss
Firing Signal
SW(fast)
I_{Total}
V_{out}
R_{Load}
C1
Vss

FIGURE 7

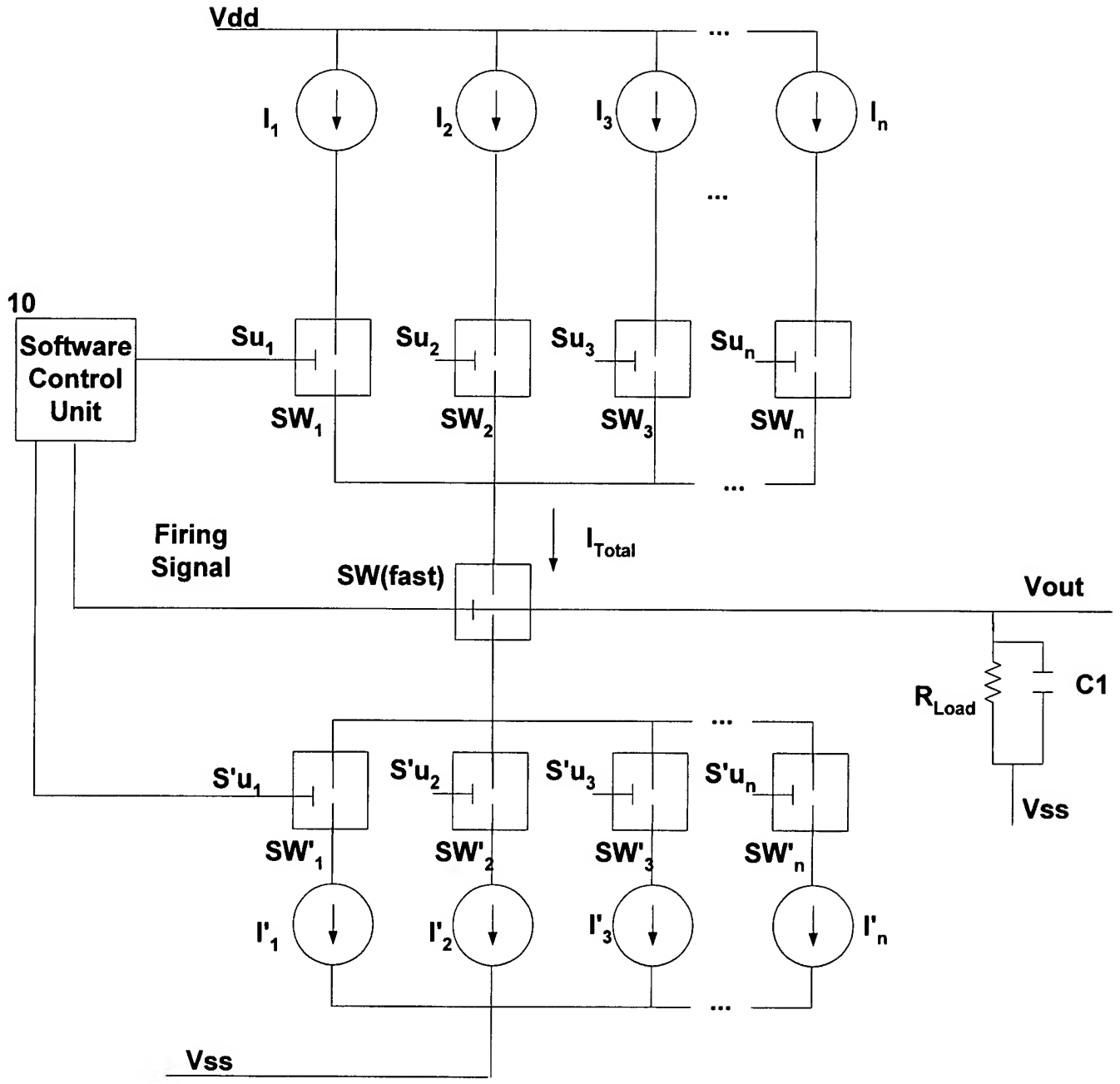
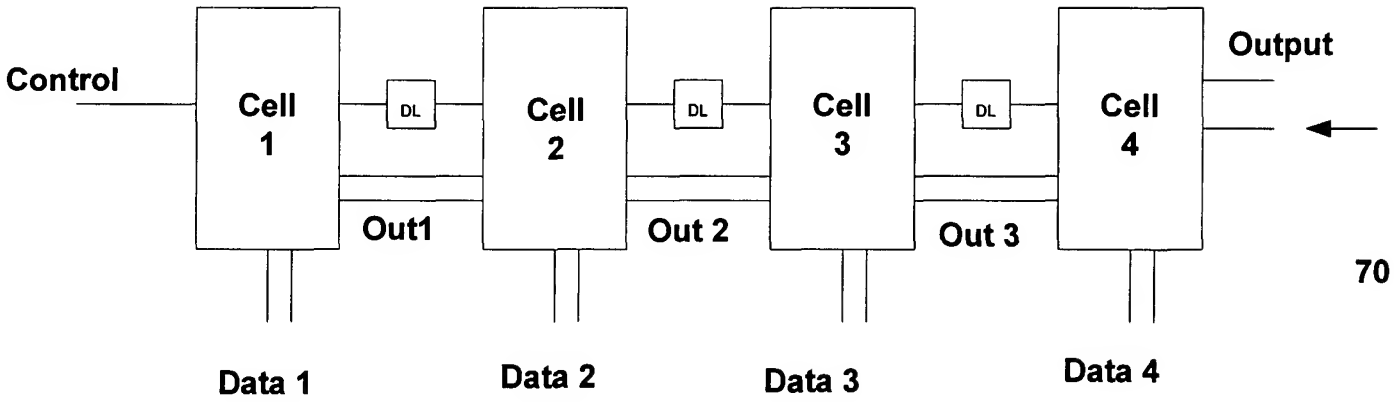

Vdd
I1
I2
I3
In
10
Software Control Unit
Su1
Su2
Su3
Sun
SW1
SW2
SW3
SWn
Firing Signal
ITotal
SW(fast)
Vout
RLoad
C1
S'u1
S'u2
S'u3
S'un
SW'1
SW'2
SW'3
SW'n
I'1
I'2
I'3
I'n
Vss
Vss

FIGURE 8


Control
Cell 1
DL
Cell 2
DL
Cell 3
DL
Cell 4
Output
Out1
Out 2
Out 3
70
Data 1
Data 2
Data 3
Data 4

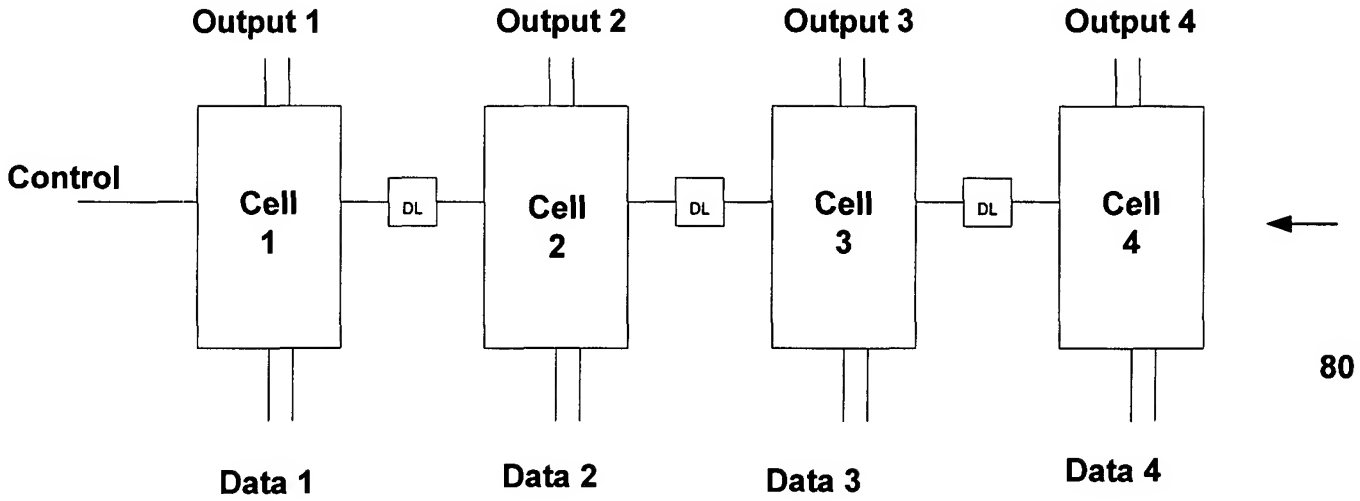

Output 1
Output 2
Output 3
Output 4
Control
Cell 1
DL
Cell 2
DL
Cell 3
DL
Cell 4
80
Data 1
Data 2
Data 3
Data 4

FIGURE 9

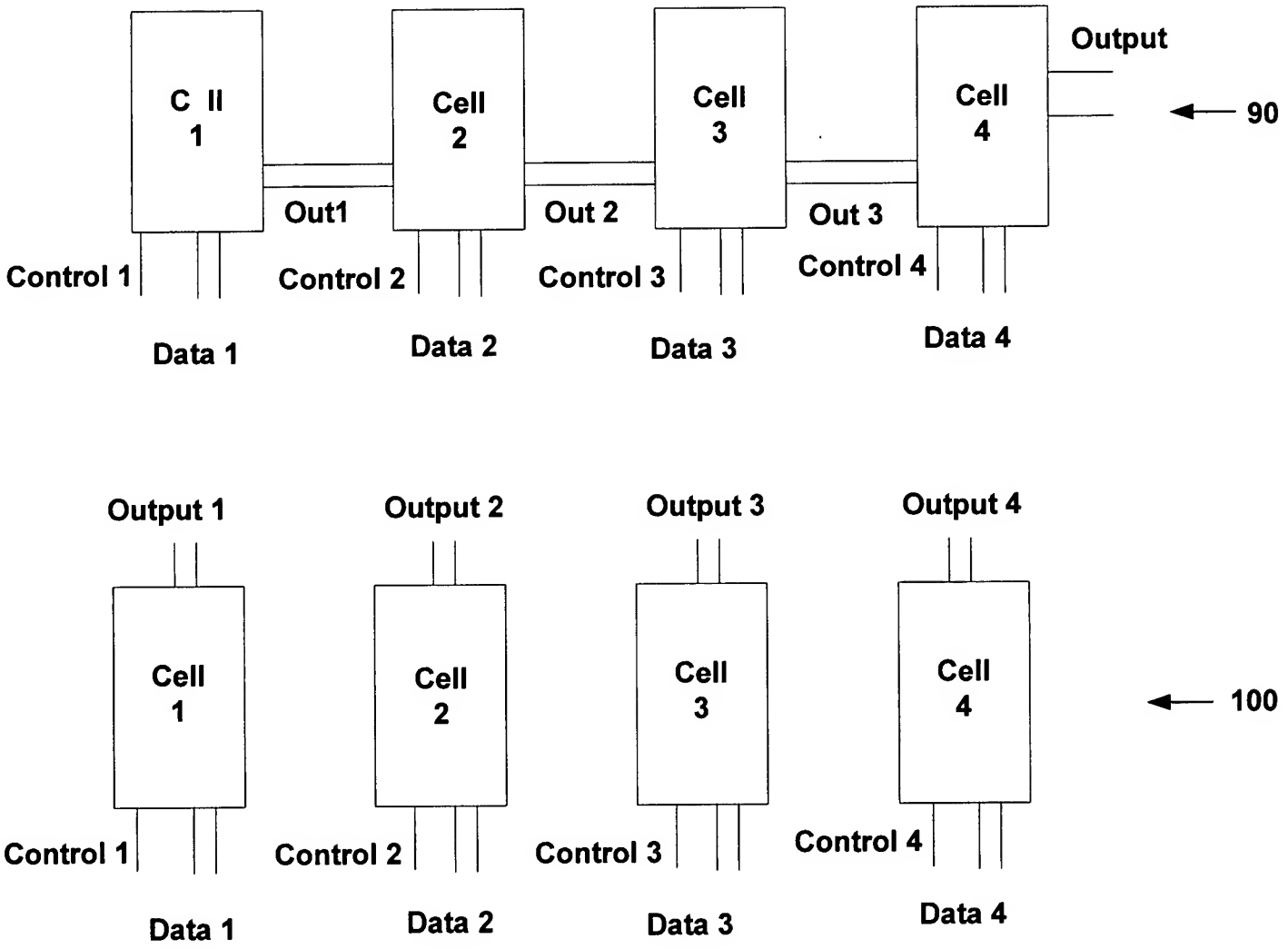

C II
1
Cell
2
Cell
3
Cell
4
Output
90
Out1
Out 2
Out 3
Control 1
Control 2
Control 3
Control 4
Data 1
Data 2
Data 3
Data 4
Output 1
Output 2
Output 3
Output 4
Cell
1
Cell
2
Cell
3
Cell
4
100
Control 1
Control 2
Control 3
Control 4
Data 1
Data 2
Data 3
Data 4

FIGURE 10

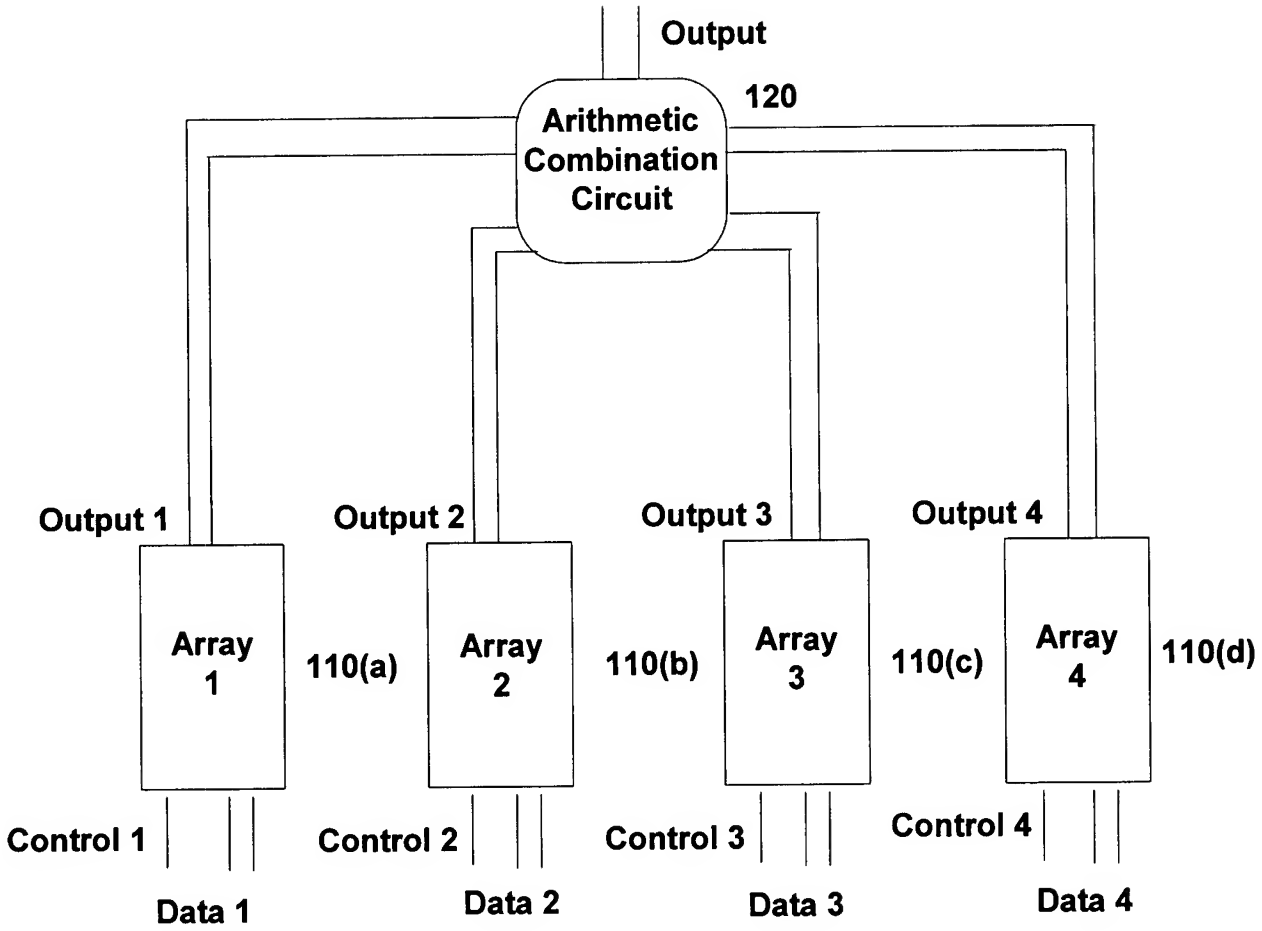

Output
120
Arithmetic Combination Circuit
Output 1
Output 2
Output 3
Output 4
Array 1
110(a)
Array 2
110(b)
Array 3
110(c)
Array 4
110(d)
Control 1
Control 2
Control 3
Control 4
Data 1
Data 2
Data 3
Data 4

FIGURE 11

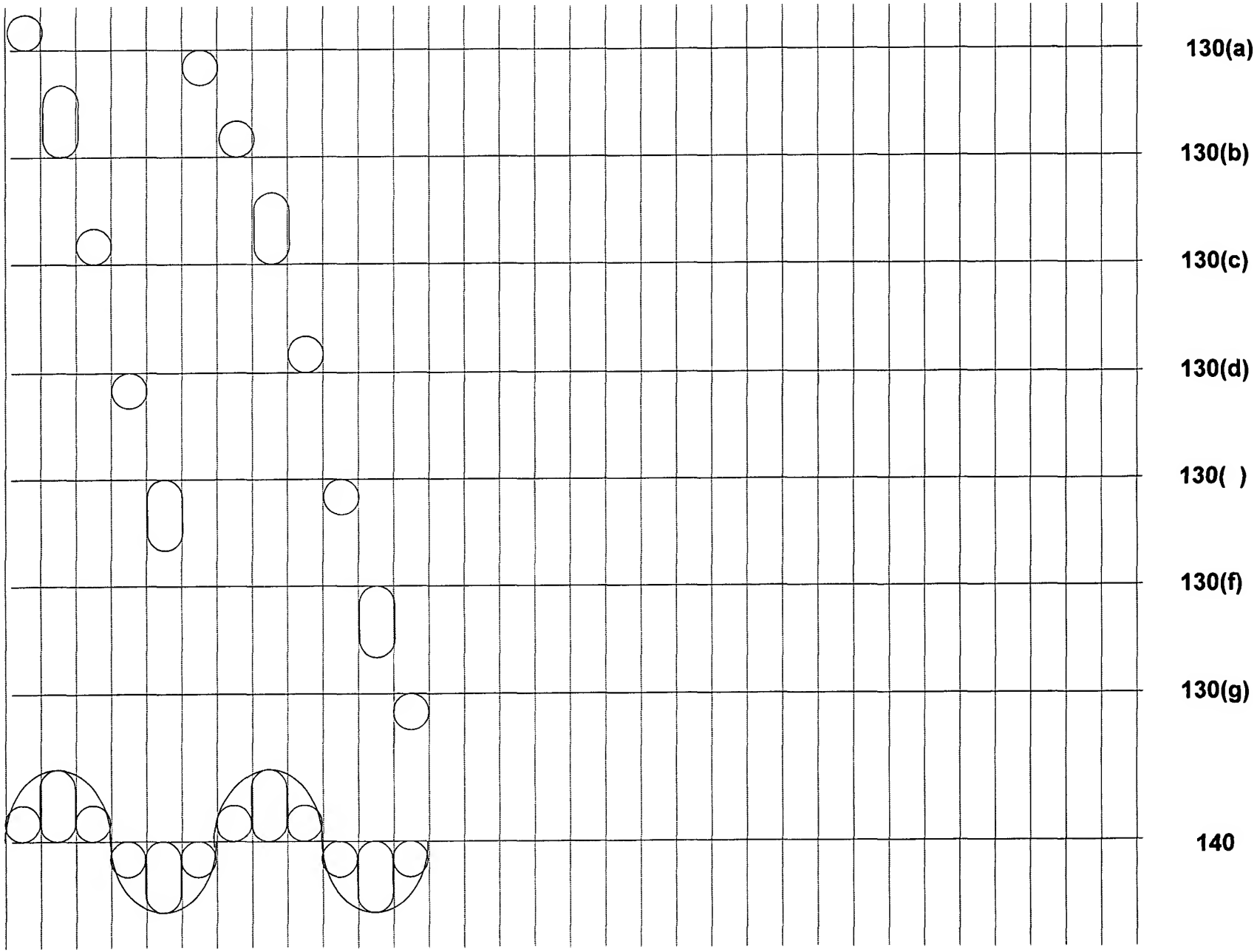
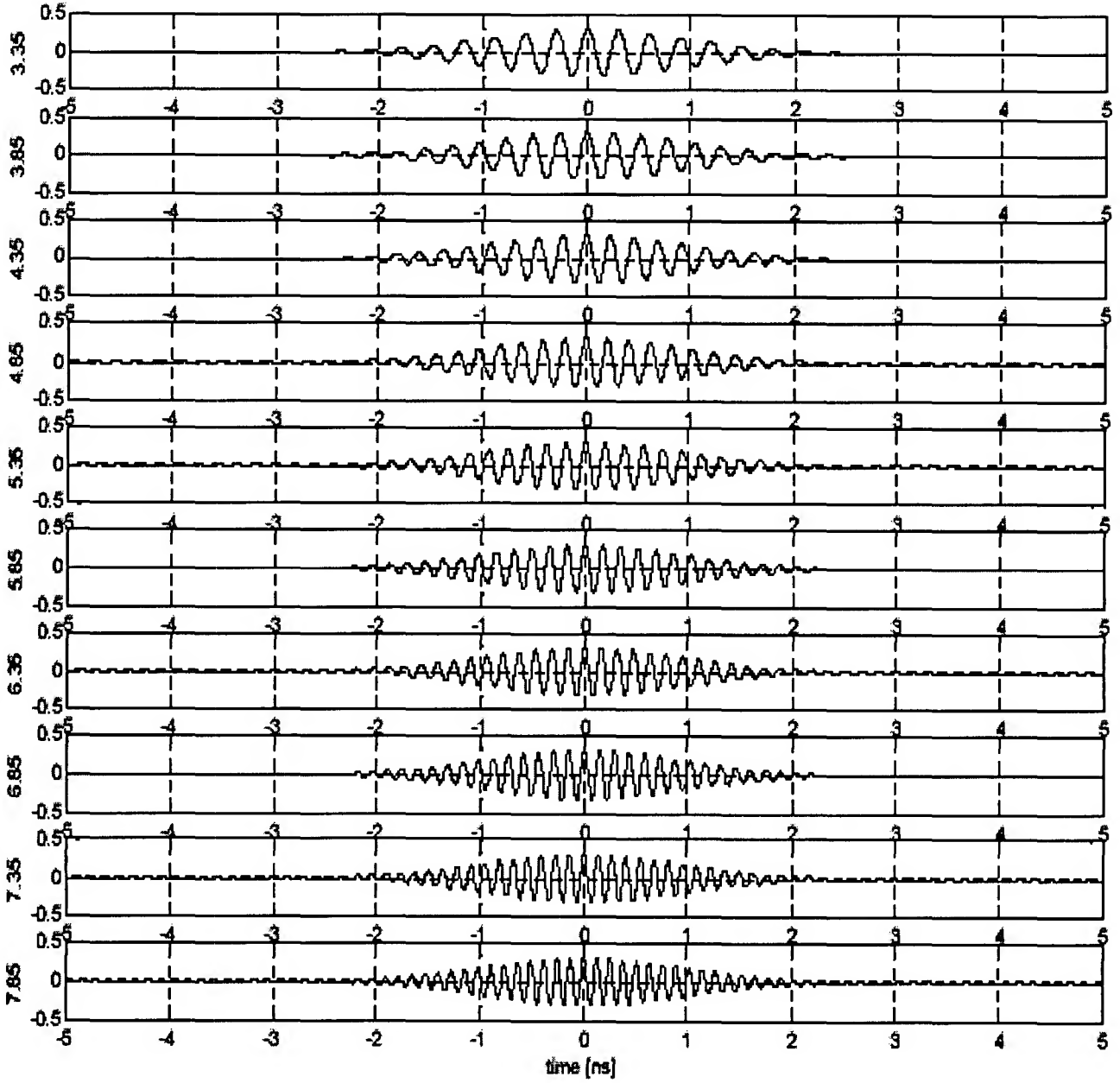


FIGURE 12



150(a)

150(b)

150(c)

150(d)

150( )

150(f)

150(g)

150(h)

150(i)

150(j)

FIGURE 13

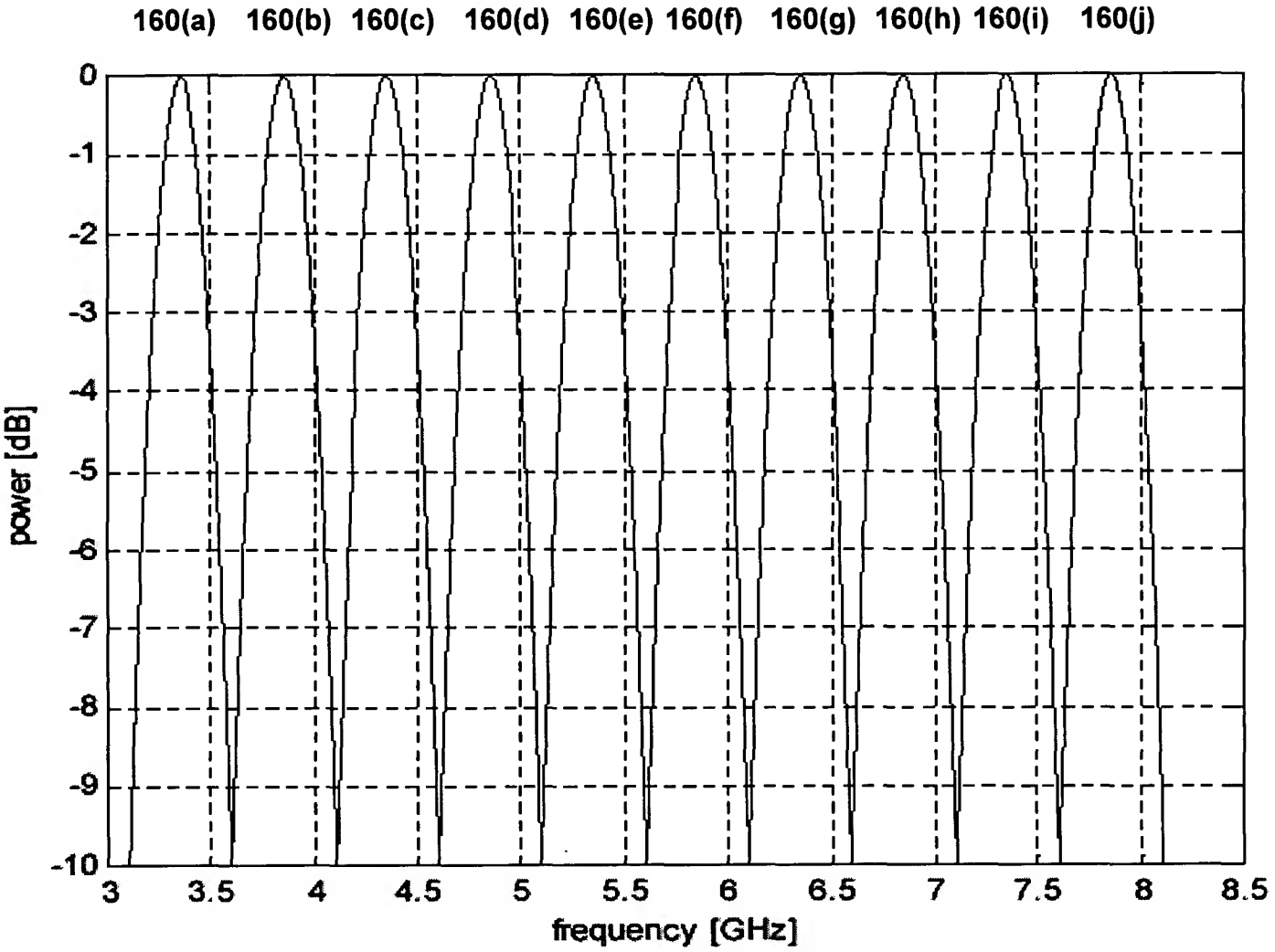

160(a)
160(b)
160(c)
160(d)
160(e)
160(f)
160(g)
160(h)
160(i)
160(j)
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
power [dB]
3
3.5
4
4.5
5
5.5
6
6.5
7
7.5
8
8.5
frequency [GHz]

FIGURE 14

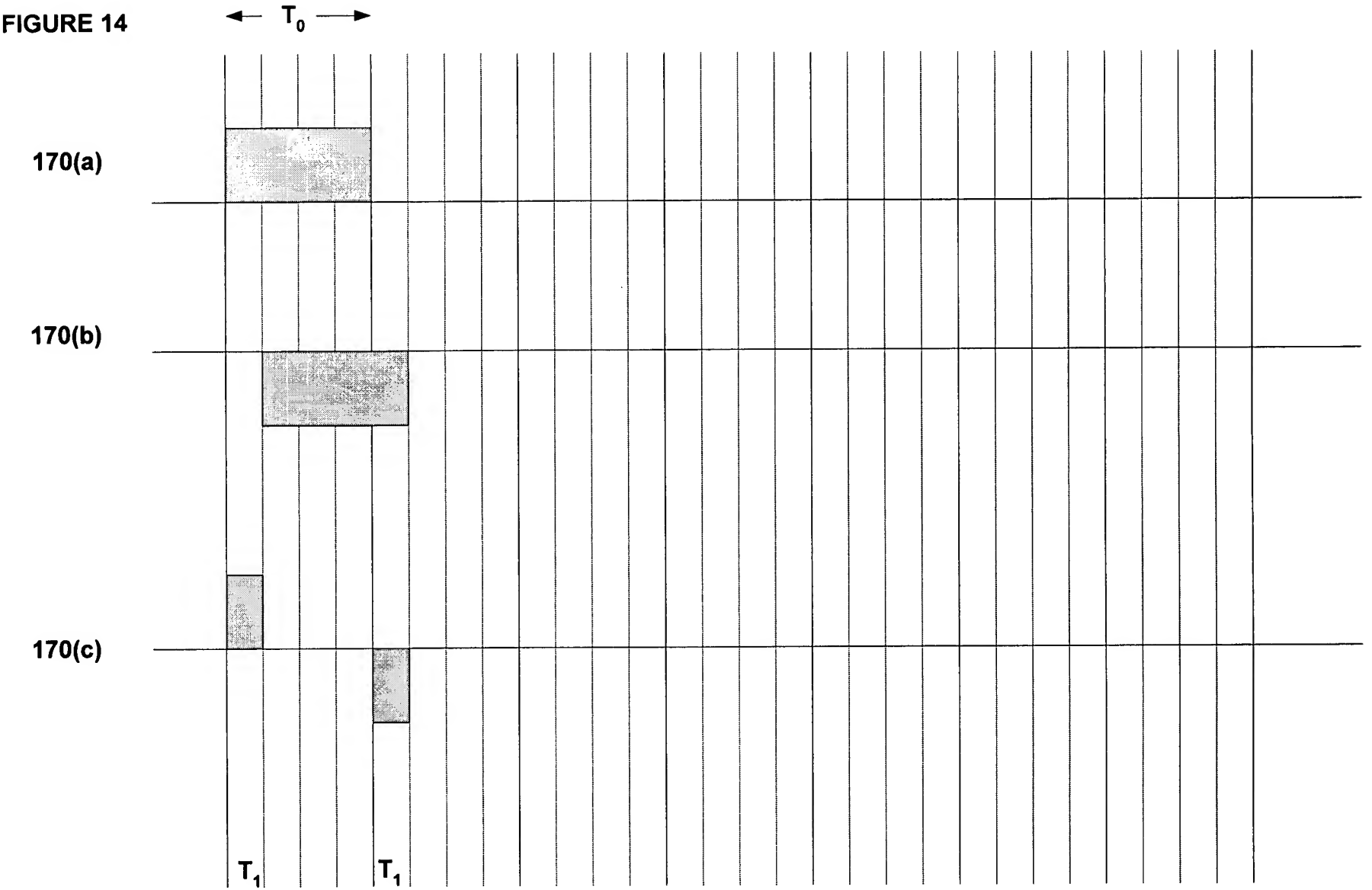


FIGURE 15

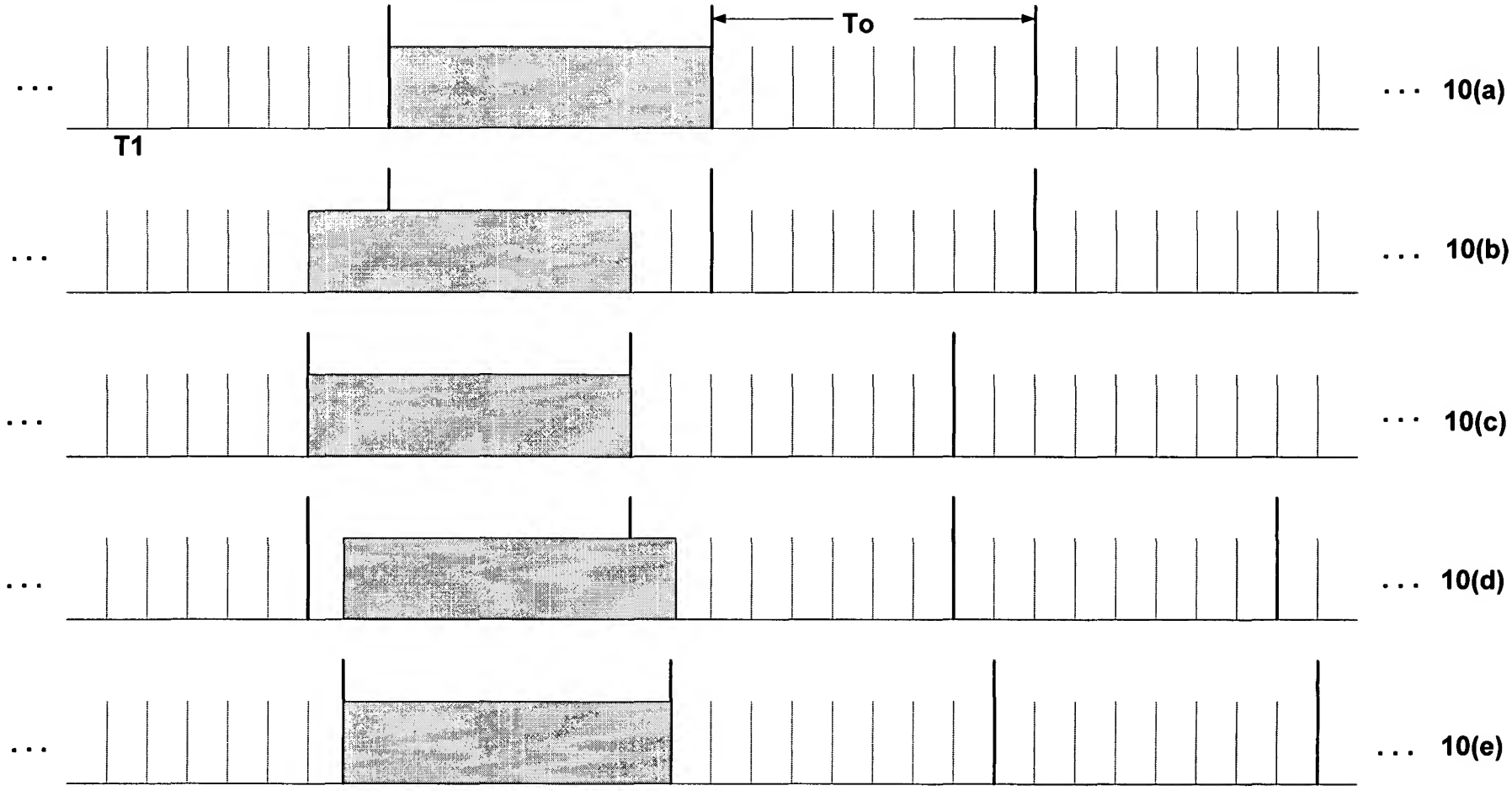
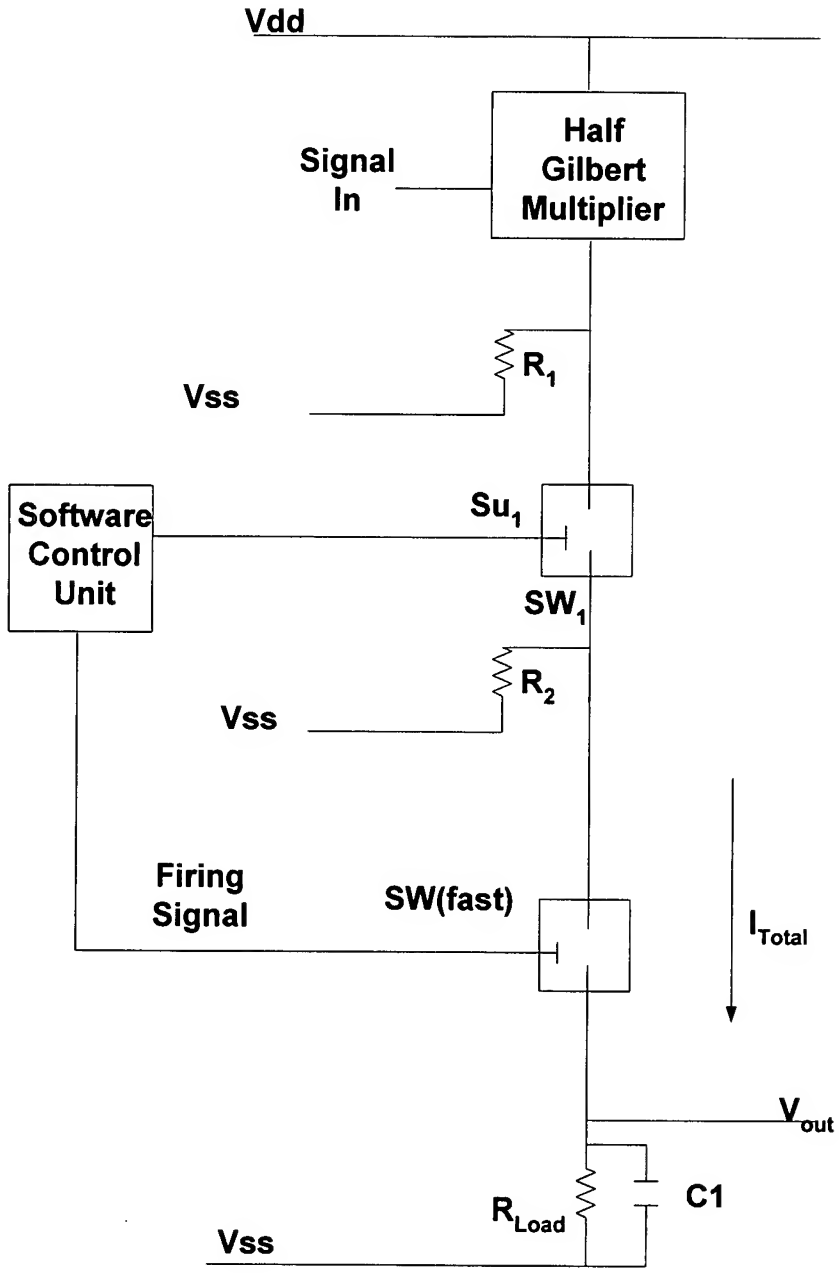


FIGURE 16


Vdd
Signal In
Half Gilbert Multiplier
R1
Vss
Software Control Unit
Su1
SW1
R2
Vss
Firing Signal
SW(fast)
ITotal
Vout
RLoad
C1
Vss